Fabrication process of Al small Josephson junctions for quantum bits

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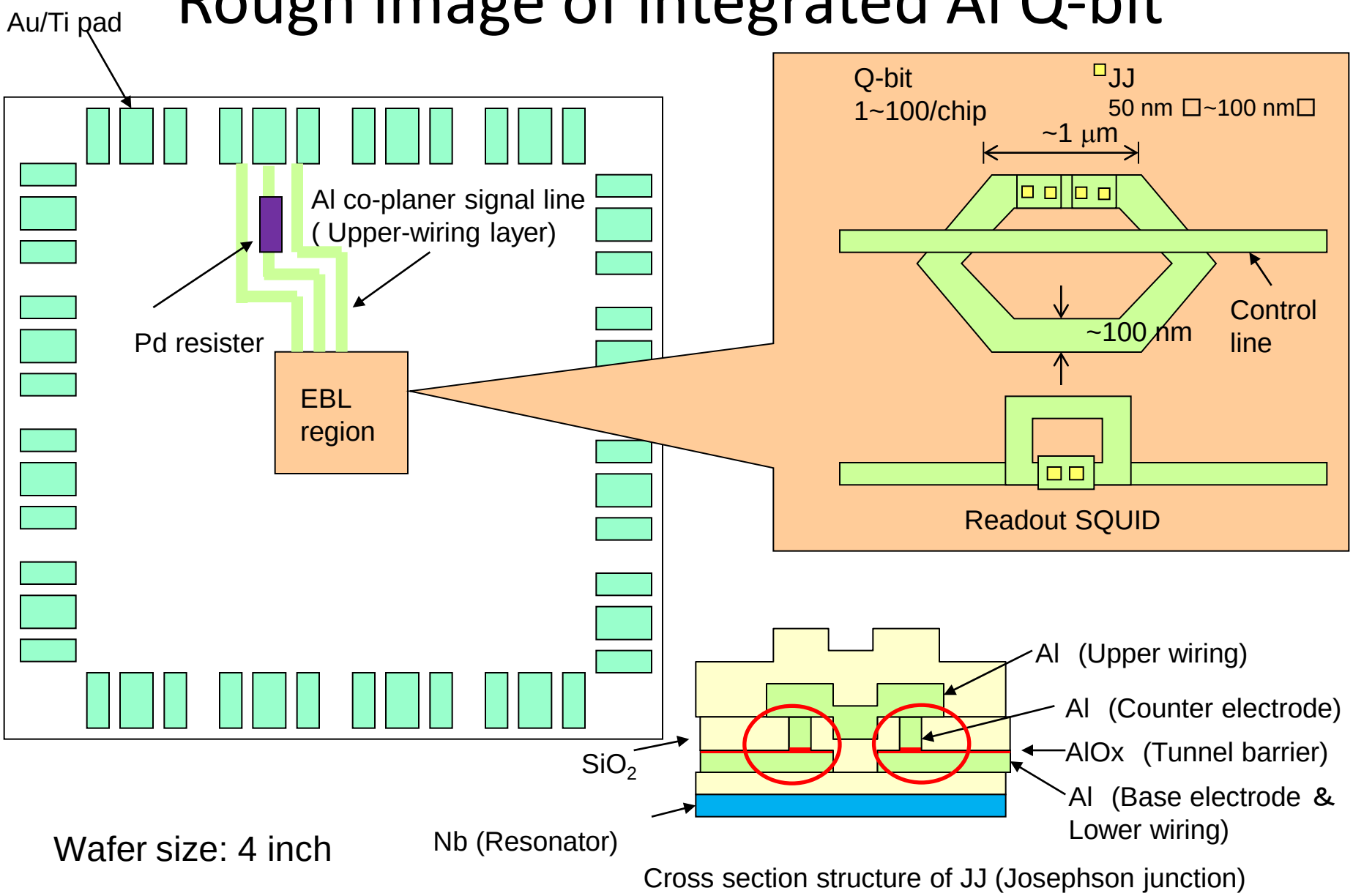
NTT: T. Maruyama

Rough image of integrated Al Q-bit



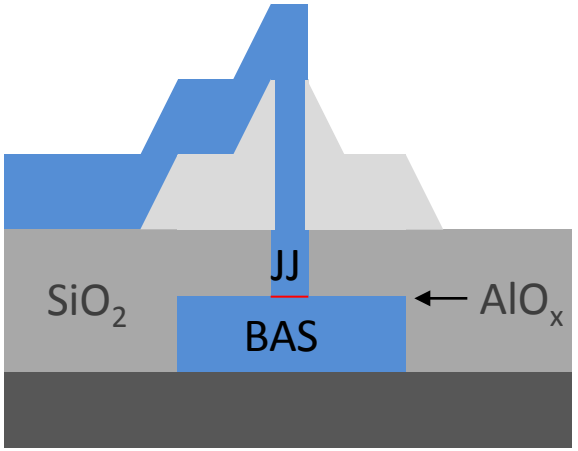
Wafer size: 4 inch

First step: fabrication of Al small (~50 nm) Josephson junctions

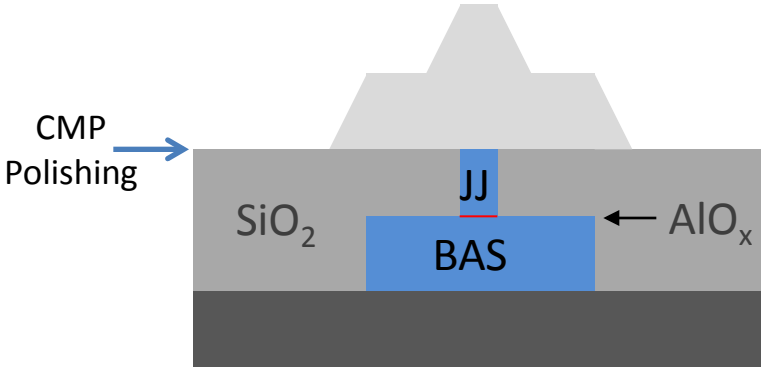
Challenges

- Deposition of smooth and grain size controlled Al.
- Patterning of small JJs(~50 nm).
- Etching Al small JJs by Chlorine RIE.
- Contact formation between JJs and the counter electrode.
- Etc.

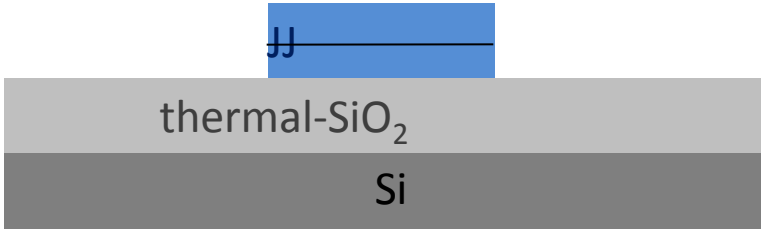
Conventional Contact through Via-hole



Contact Formation by using CMP
= Exposure of Counter Electrode of JJ



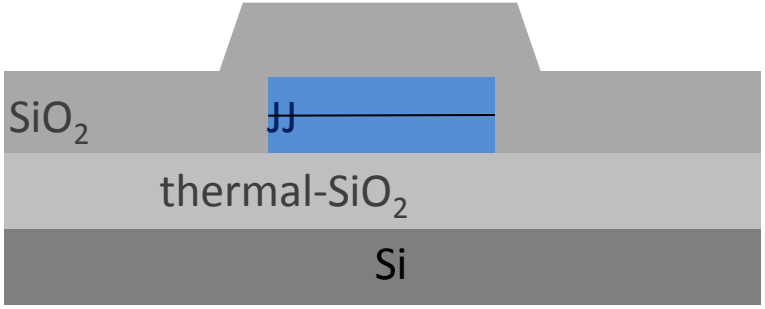
Contact Formation



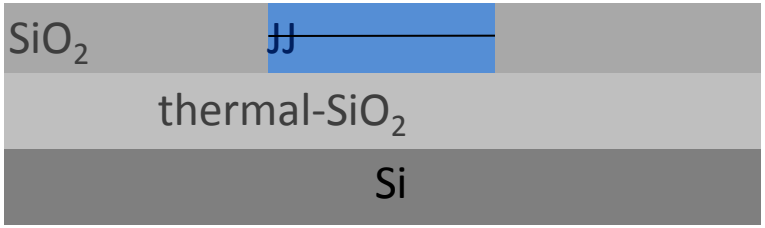
Process sequence

trilayer deposition
(dc magnetron sputtering)

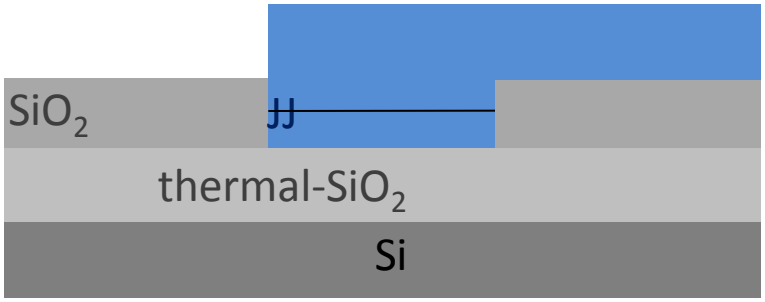
etching



SiO_2 deposition
(bias sputtering)



CMP

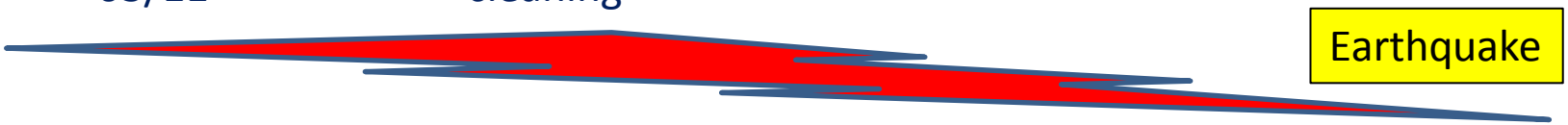


COU deposition
(dc magnetron sputtering)

etching

Al JJ Process Ver. 1

01/late	CAD data + Al/AlO_x/Al films sent to SCR
	JJ: EB lithography + etching + cleaning
02/25	wafers sent to ISTEC
02/28-03/03	BAS: EB lithography + dev.
03/07	BAS etching + cleaning
03/07	SiO_2 deposition
03/08	CMP
03/08	COU: Al deposition
03/09	alignment window: EB lithography + dev. + etching
03/11	cleaning



03/30	wafer sent to Maruyama-san NTT
May	COU: EB lithography + dev. + etching + cleaning dicing
	Characterization: I-V, SEM, (TEM)

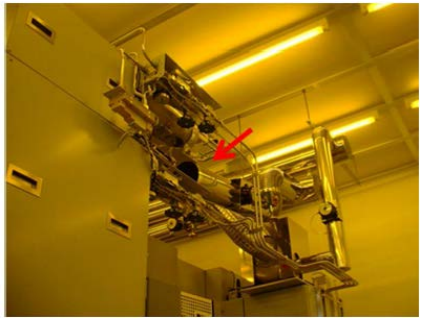
Damage by the earthquake

- Unplanned stop of machines
- Mechanical damage to buildings/machines

  - some need repairing
- Limited electricity supply

  - no air-conditioning in cleanrooms
- Leakage in waste-water pipelines

  in Tsukuba Central area

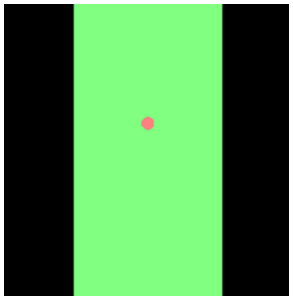


Al JJ Process Ver. 1
CAD Pattern

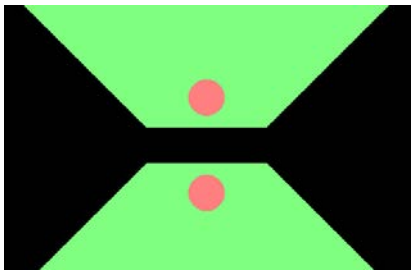
JJ-1 chip
JJ size (from left to right)
- 0.1 μm x 2
- 0.3 μm x 2
- 0.6 μm x 2
- 1.0 μm x 2
- 3.0 μm x2
- 0.2 μm x1
- 0.4 μm x1
- 0.8 μm x1
- 2.0 μm x1

JJ-2 chip

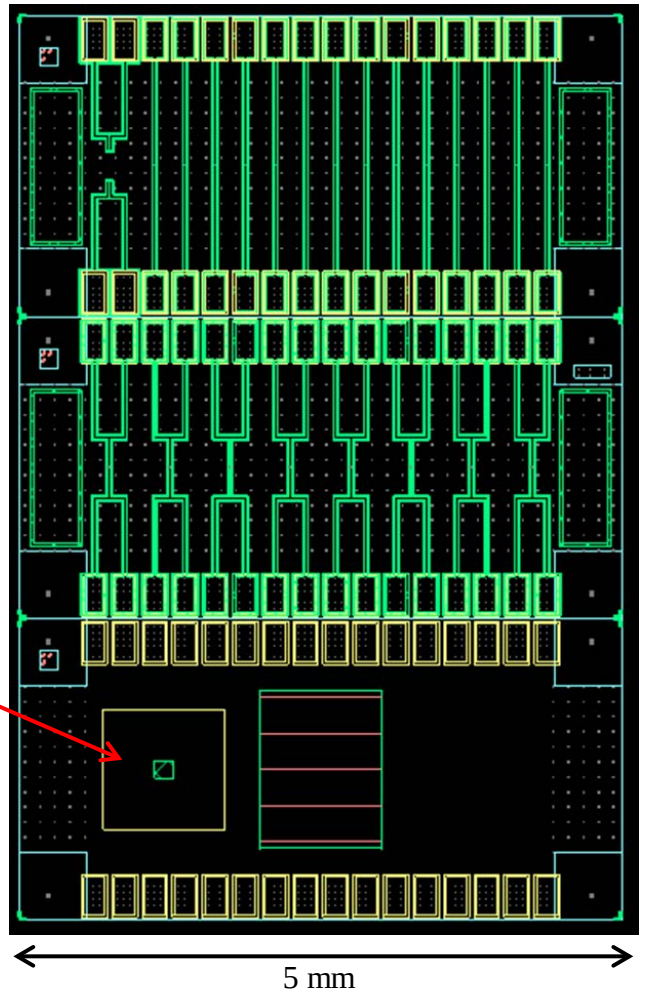
JJ size (μm)	0.8	0.3	0.8	0.3	0.8	0.3	0.8	0.3
JJ distance (μm)	2.0	2.0	1.5	1.5	1.0	1.0	0.5	0.5
COU gap (μm)	1.0	1.0	1.0	1.0	0.8	0.8	0.3	0.3

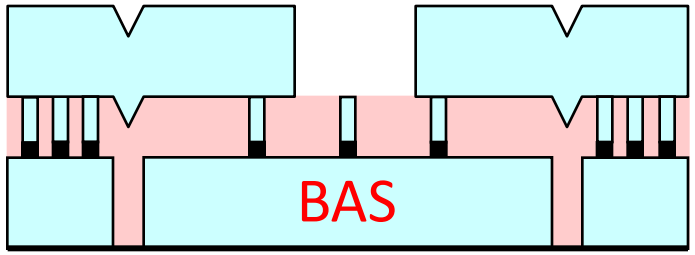


JJ-1



JJ-2



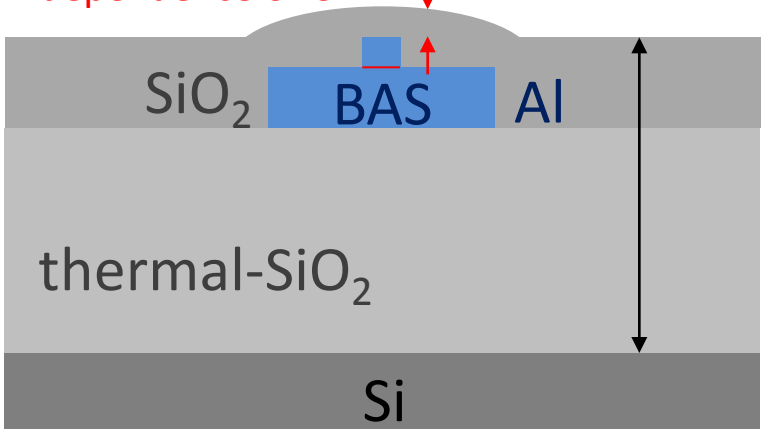


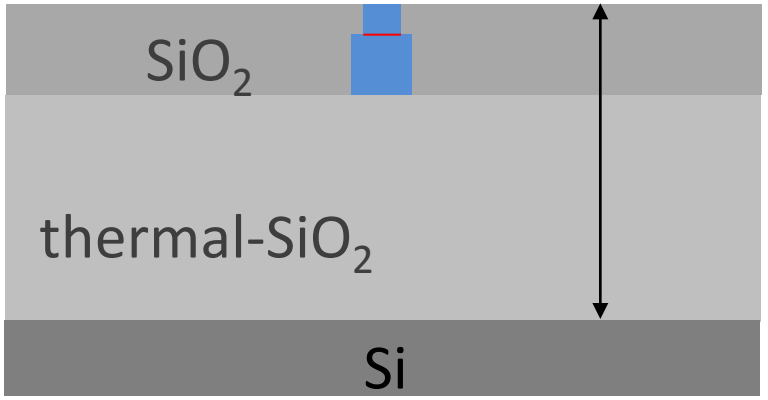
Endpoint Detection Trouble

Pattern Size Dependence of CMP

Pattern in Process Ver. 1

height difference due to pattern-size-dependence of CMP

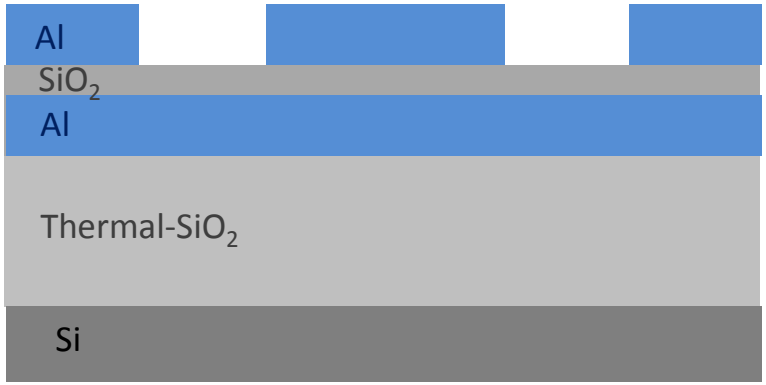


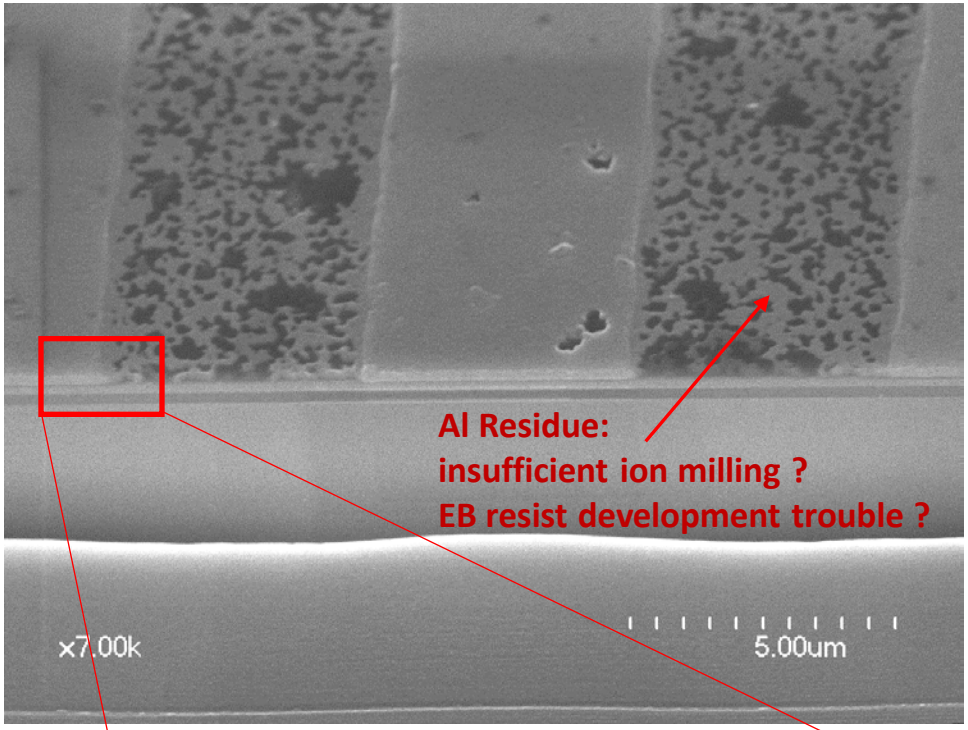


BAS Pattern: too large
Endpoint Detection Trouble

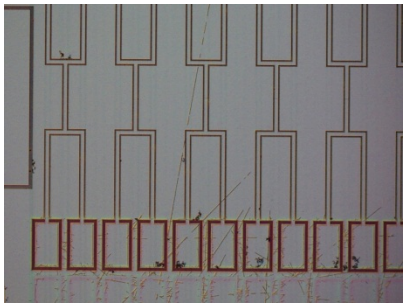
➔ Under-polished or Over-polished CMP

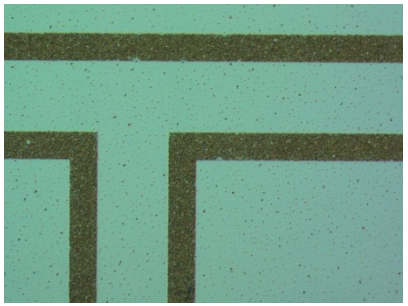
Al-JJ Cross-sectional SEM (SCR: Yamagishi)

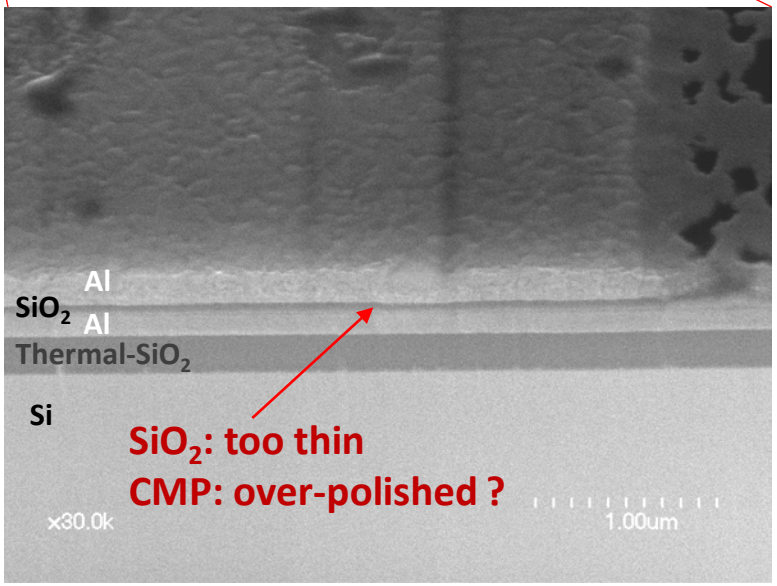




Optical Micrograph (NTT)

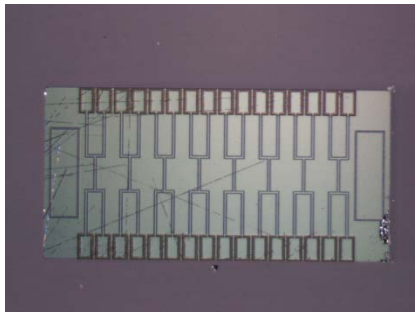


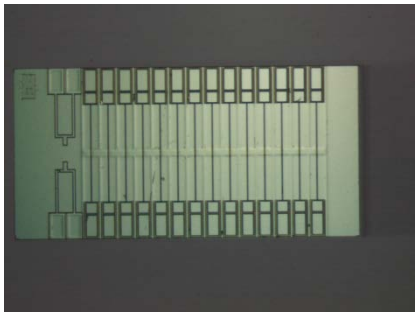




Characterization (NTT)

Optical Micrograph after Dicing

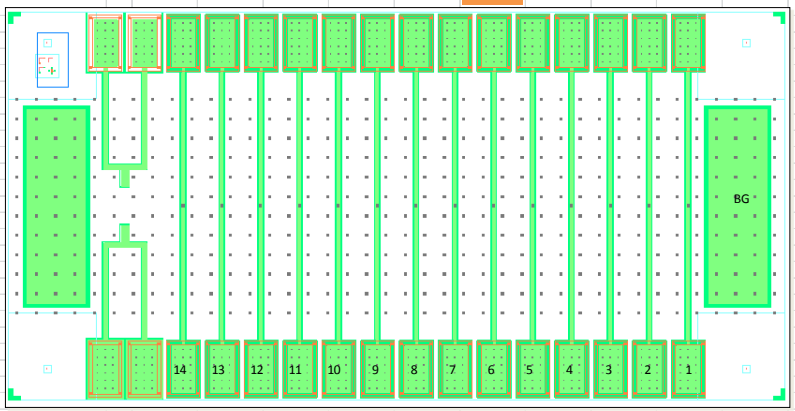




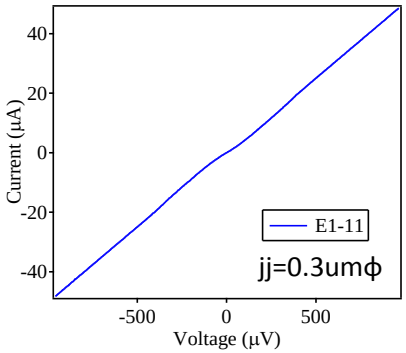
2-probe Measurement at R.T.

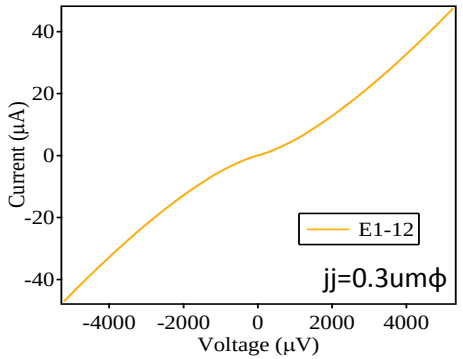
JJ-BG 室温測定値
※測定系の抵抗値：4Ω程度

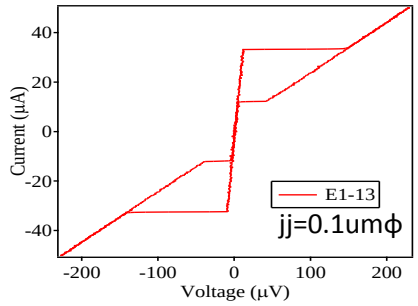
	JJ径	A1	C1	C2	C3	E1	E2	E3
1	2.0	3.89	8.18	7.73	5.88	25.19	9.12	3.91
2	0.8	3.88	8.57	8.56	6.16	16.64	4.26	3.91
3	0.4	3.89	8.53	9.04	6.56	25.58	6.35	3.91
4	0.2	4.29	10.17	8.73	5.37	26.60	4.05	3.91
5	3.0	3.91	9.91	6.83	6.16	30.12	3.77	3.91
6	3.0	4.22	9.06	8.52	6.80	16.00	17.64	4.18
7	1.0	4.20	6.88	7.16	6.41	30.12	5.86	3.91
8	1.0	5.19	9.77	6.35	6.22	20.62	4.31	3.92
9	0.6	5.15	5.07	6.09	5.85	28.49	4.03	7.65
10	0.6	5.07	9.94	6.23	6.72	29.76	3.91	13.07
11	0.3	5.00	10.73	7.13	5.99	39.68	5.09	3.92
12	0.3	4.98	10.60	6.83	5.28	16.67	3.91	3.92
13	0.1	6.10	10.78	7.08	7.14	41.67	9.47	3.92
14	0.1	5.93	9.91	7.31	6.47	36.10	3.91	7.24

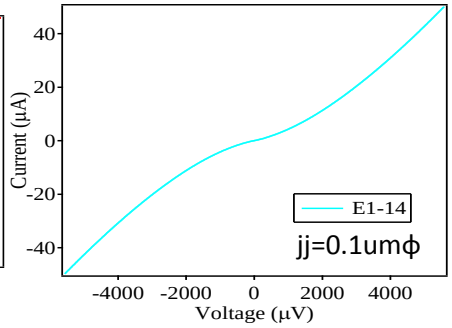


4-probe Measurement at T = 14 mK
E1 chip









Next Process Ver. 2

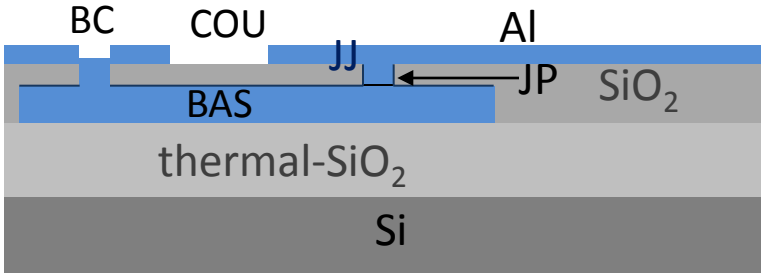
We need

- Design: Small BAS Pattern

  to ensure end-point detection of CMP

- Ion Milling Optimization

- Readjustment of fabrication machines

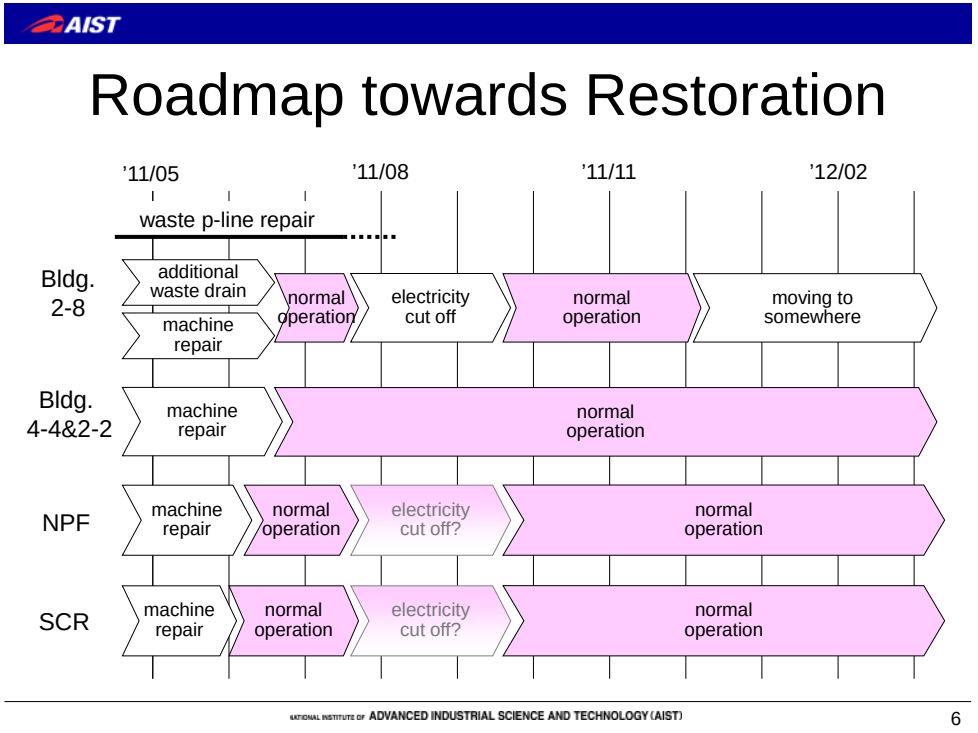


Process Sequence	No.1	No.2
1) Trilayer Deposition (ISTEC)	✓	✓
2) JJ Etching (SCR)	✓	✓
3) JJ Protection (JP) Layer		✓
4) BAS Etching (SCR)	✓	✓
5) SiO_2 Deposition (SCR or ISTEC)	✓	✓
6) CMP (ISTEC)	✓	✓
7) BC contact Etching (NPF/ISTEC)		✓
8) COU deposition (ISTEC)	✓	✓
9) COU Etching (NPF/ISTEC)	✓	✓

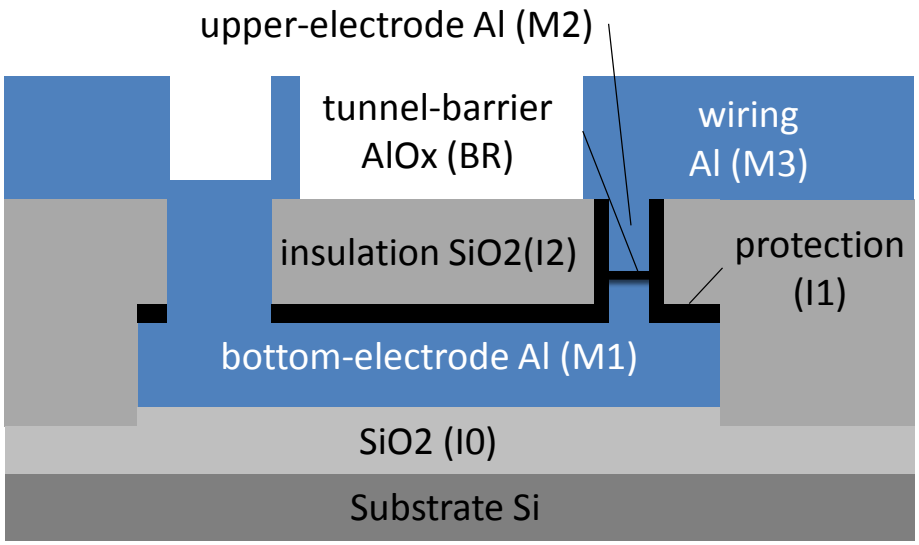
3) JJ Protection Layer : PCVD SiO_2 or Anordization
5) SiO_2 Deposition : PCVD SiO_2 or Bias-sputter SiO_2

AIST facilities: status quo

- Clean rooms restarted at the end of July
- No long-term electricity cut-off
- No more electricity-saving requirement
- Restoration of most facilities and machines
- Condition changes for some machines → re-adjustment



Al/AlOx/Al JJ process ver. 2



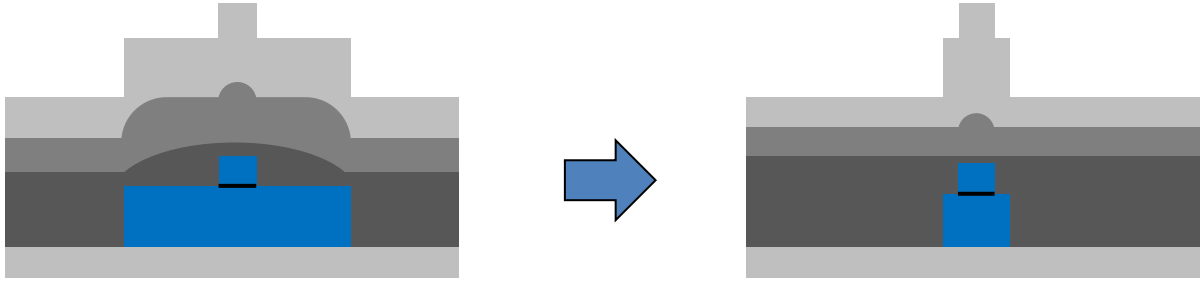
layer	material	thickness	method
I0	SiO2	300 nm	therm-oxid.
M1	Al	200 nm	sputtering
BR	AlOx	~1 nm	therm-oxid.
M2	Al	100 nm	sputtering
I1	(a) SiO2 (b) AlOx	50 nm 10 nm	PECVD anodization
I2	SiO2	500 nm	(a)PECVD (b)sputtering
M3	Al	150 nm	sputtering

- Feedback from ver. 1
  bottom-electrode design, wiring layer etch
- Other improvements
  protection layer, PECVD SiO2, resist slimming
- Parallel processing of 2 variants (ver. 2-a/2-b)

Ver. 2: improvements (1)

- Narrow bottom electrode design

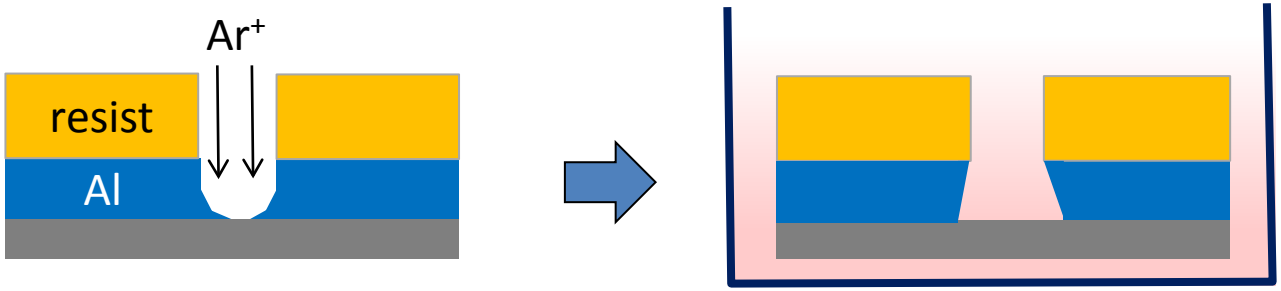
  → uniform planarization



- Wiring layer (M3) etch:

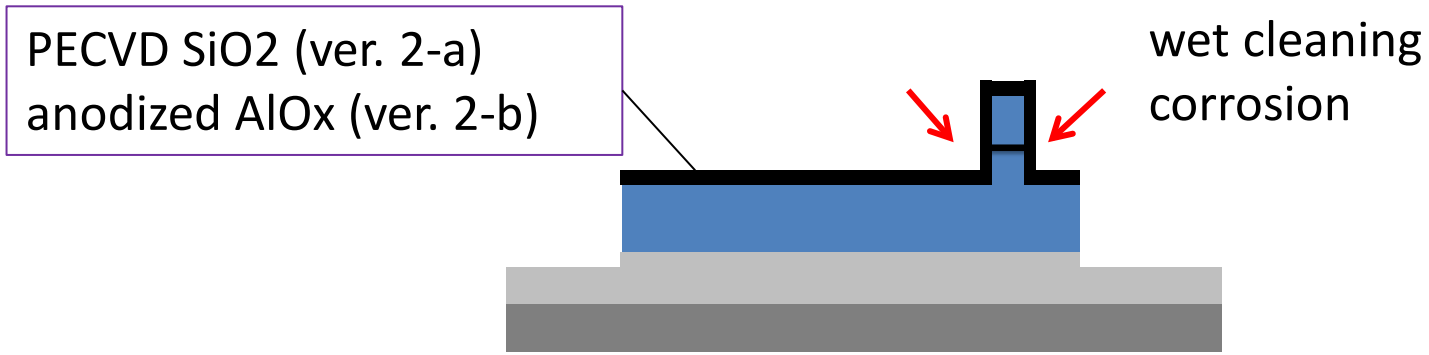
  - optimum ion-milling condition

  - additional wet etch after ion-milling



Ver. 2: improvements (2)

- Additional protection layer



- Plasma enhanced CVD (PECVD) SiO2 (Ver. 2-a)
  - better coverage, lower defect-density
  - low growth temperature < 250C
    (cf. ~350C for standard semiconductor process)

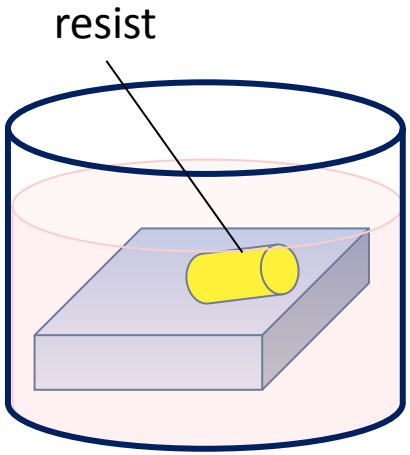
Ver. 2: improvements (3)

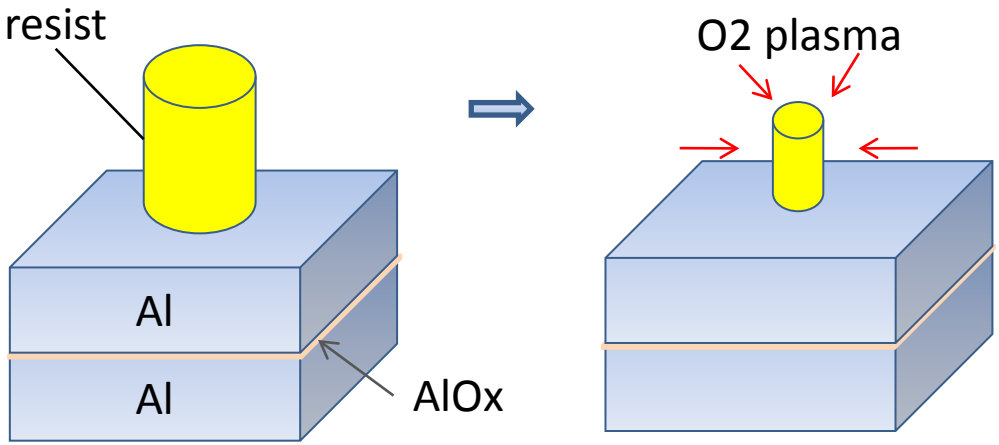
- Resist slimming technique

  high-aspect pillar-shape resist

  → tumbling during development/cleaning

  EB resist slimming by dry O2 ashing

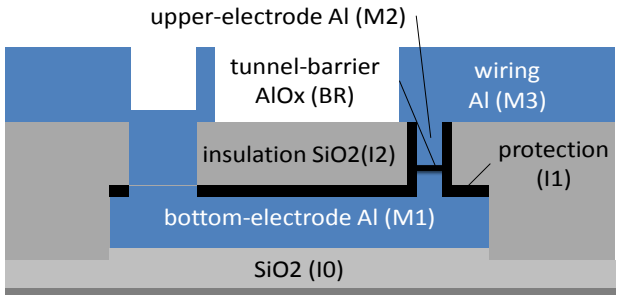




Ver. 2: process flow

Ver. 2-a

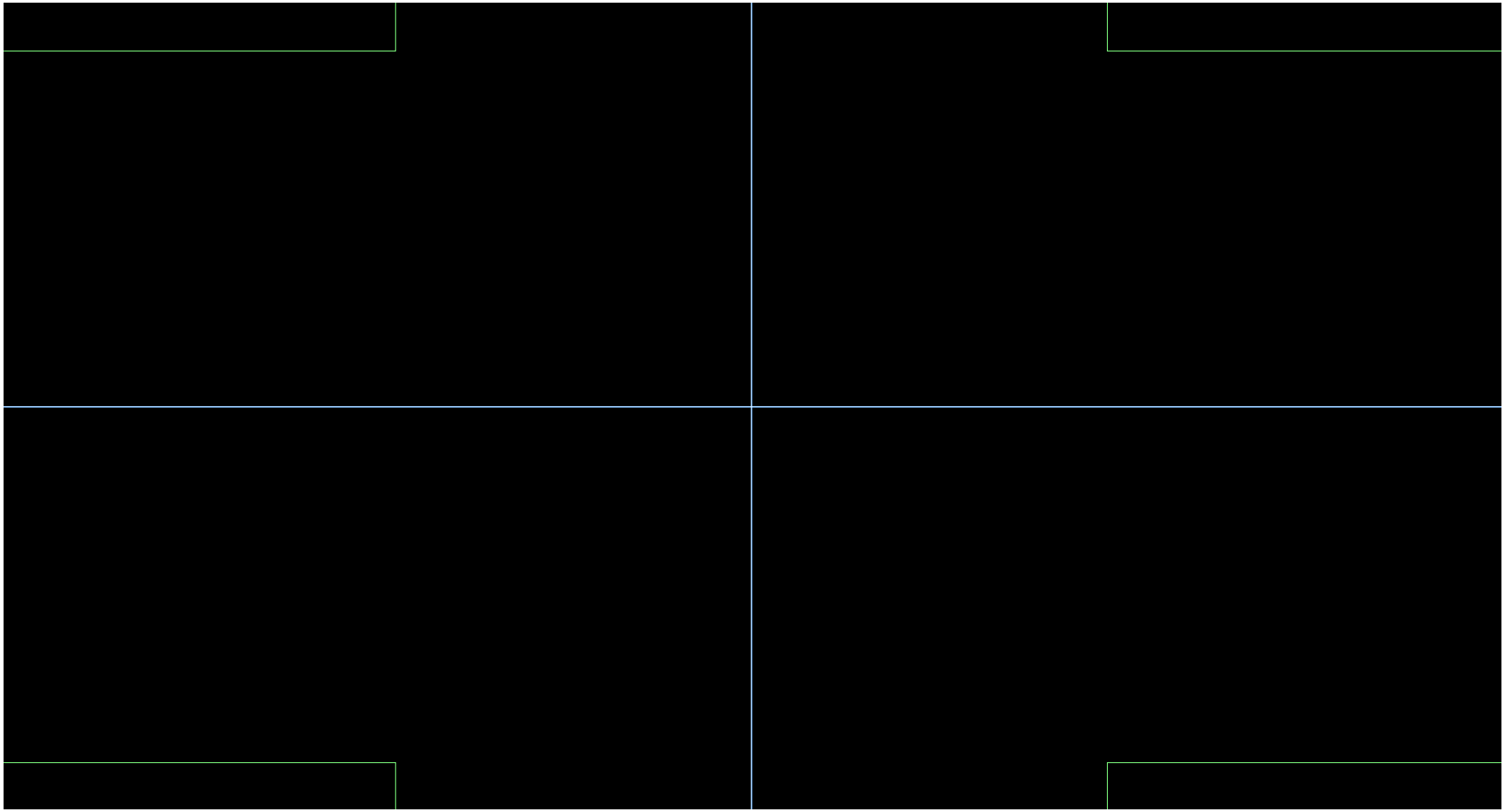
process	facility
(1) Al/AlOx/Al deposition	SCR
(2) u-electrode patterning	
(3) protection layer deposition PECVD SiO2	
(4) b-electrode patterning	
(5) insulation layer deposition PECVD SiO2	
(6) planarization	Bldg. 4-4
(7) via-hole patterning	NPF Bldg. 2-8
(8) wiring deposition	
(9) wiring patterning	NPF Bldg. 4-4



Ver. 2-b

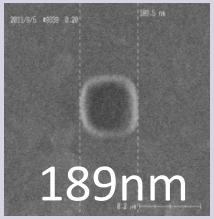
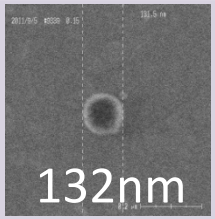
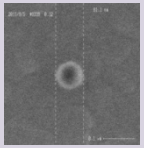
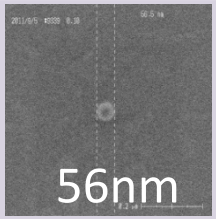
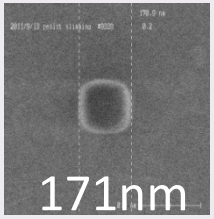
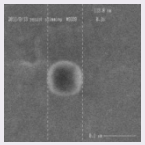
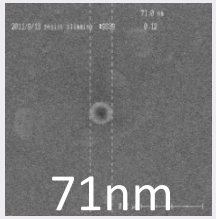
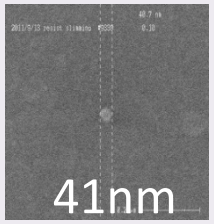
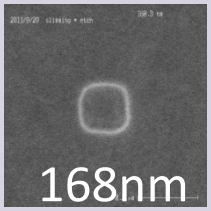
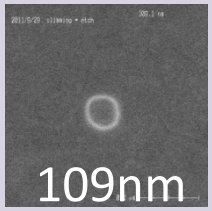
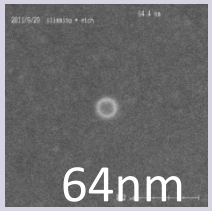
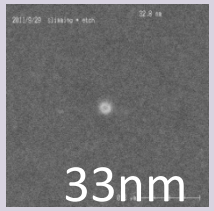
process	facility
(1) Al/AlOx/Al deposition	SCR
(2) u-electrode patterning	
(3) protection layer deposition anodized AlOx	Bldg. 4-4
(4) b-electrode patterning	NPF Bldg. 4-4
(5) insulation layer deposition sputtered SiO2	Bldg. 4-4
(6) planarization	
(7) via-hole patterning	NPF Bldg. 2-8
(8) wiring deposition	
(9) wiring patterning	NPF Bldg. 4-4

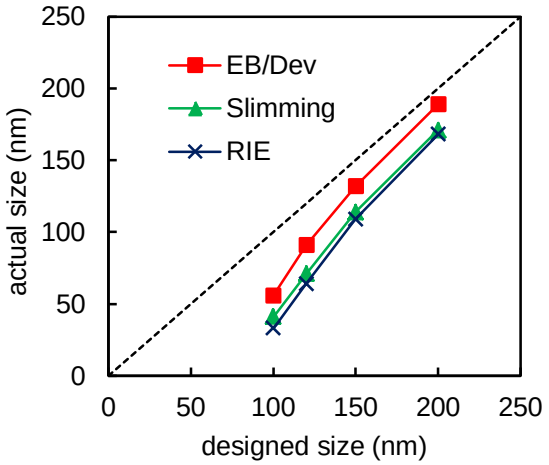
Mask design



Preliminary result

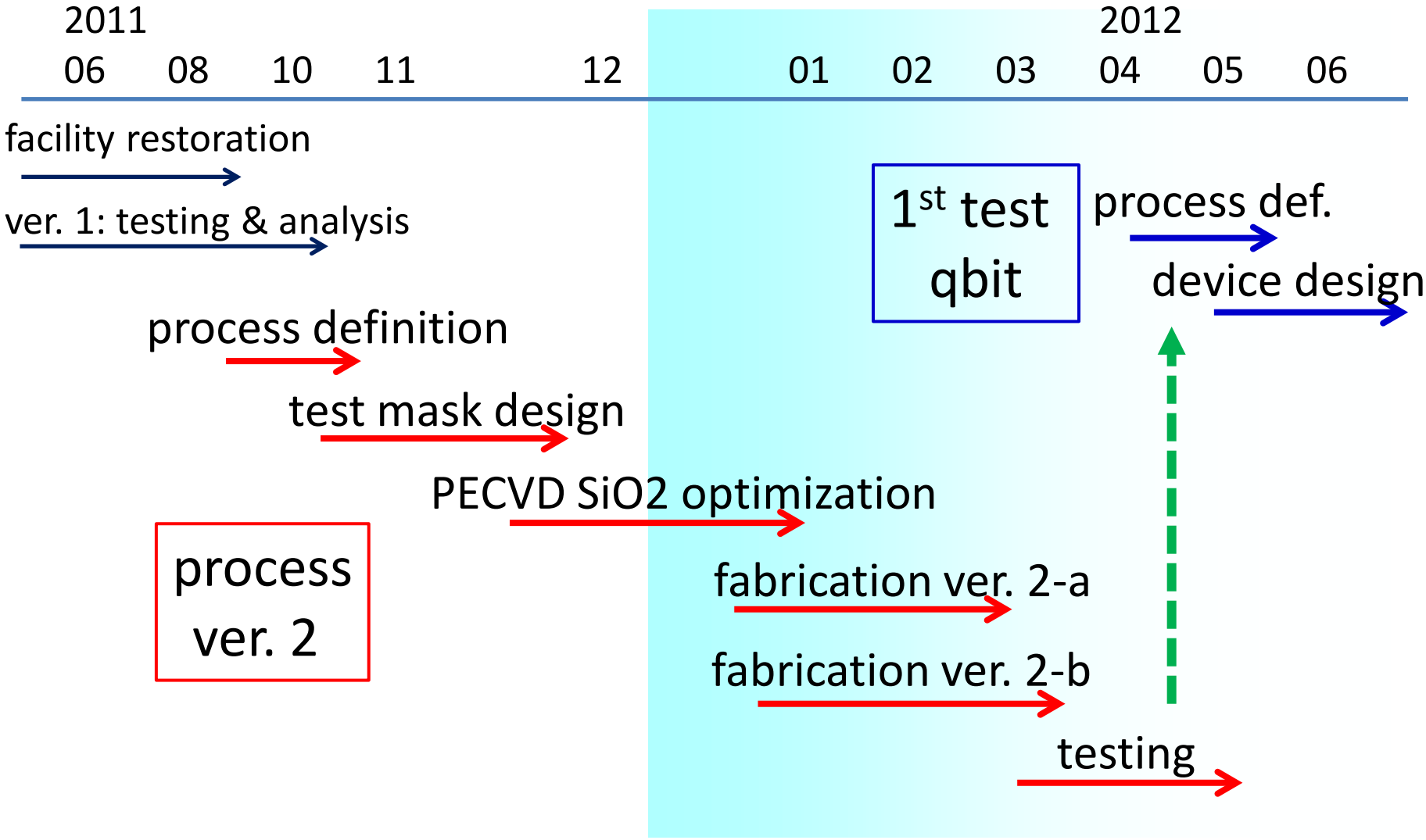
Al patterning with resist slimming

Design	200nm	150nm	120nm	100nm
after EBL/dev	 189nm	 132nm	 91nm	 56nm
after slimming (ashing)	 171nm	 114nm	 71nm	 41nm
after RIE	 168nm	 109nm	 64nm	 33nm



Successful fabrication of Al pillar with d < 50 nm

Short-term plan



Summary

- Integration technology for supercond. qbits
- Earthquake during process ver. 1
- Unsuccessful results of ver. 1
- Process improvements in ver. 2